80Gb/s Optical Packet Routing for Data Networking using FPGA Based 100Mb/s Control Scheme

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Abstract A novel router is demonstrated. Wavelength striped packets at 80Gb/s aggregate bit rate are routed with a separate 100Mb/s control channel for low cost LAN applications. An FPGA drives the broadband MZ and SOA switches.

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Introduction

Despite advances in ultrahigh capacity photonic transmission and high speed switching capabilities, obstacles remain at the electronic-photonic interface before commercial solutions can become available. In this work we address and characterise the dynamic reconfiguration of optical switch fabrics for high capacity routing using a field programmable gate array (FPGA) with commercially available photonic components.

All optical routing control schemes have been demonstrated at line rates of up to 100Gb/s [1] but with a complexity unsuited to data networking. Wavelength routing schemes operating at 2.5Gb/s per channel with 622Mb/s headers containing routing information have been demonstrated [2]. While such schemes allow the direct interfacing to high speed electronic control circuits, the advantage of high capacity is lost through the wavelength granularity.

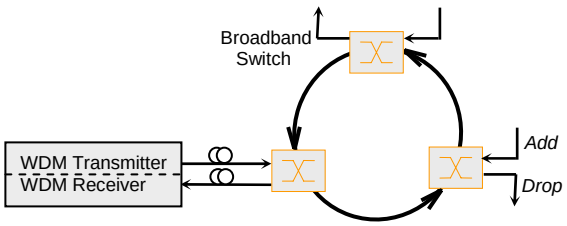


Fig.1. Ring implementation for wavelength striped high capacity routing

Implementing wavelength multiplexing in point-to-point links through byte wide transmission [3] allows an increase in capacity while using off-the-shelf transceiver technologies. In this work, we demonstrate a new network configuration whereby packets are striped across blocks of wavelengths to exploit reduced packet durations and therefore provide a route to low latency networking. The blocks of wavelengths are then switched in and out of a ring network using broadband optical switch fabrics such as Mach-Zehnder interferometers (MZ) or semiconductor optical amplifier (SOA) switches as shown in Fig.1. To facilitate control of packets with aggregate bit rates of 80Gb/s, a separate wavelength is set aside for control. The control bit rate to the switch only need operate at 100 Mb/s to facilitate addressing and switch control for multiple destinations. Full electronic control is thus demonstrated using a FPGA interfaced to the switch and control channel transceiver in a manner readily extendable to both multiple switch and multiple switch port architectures.

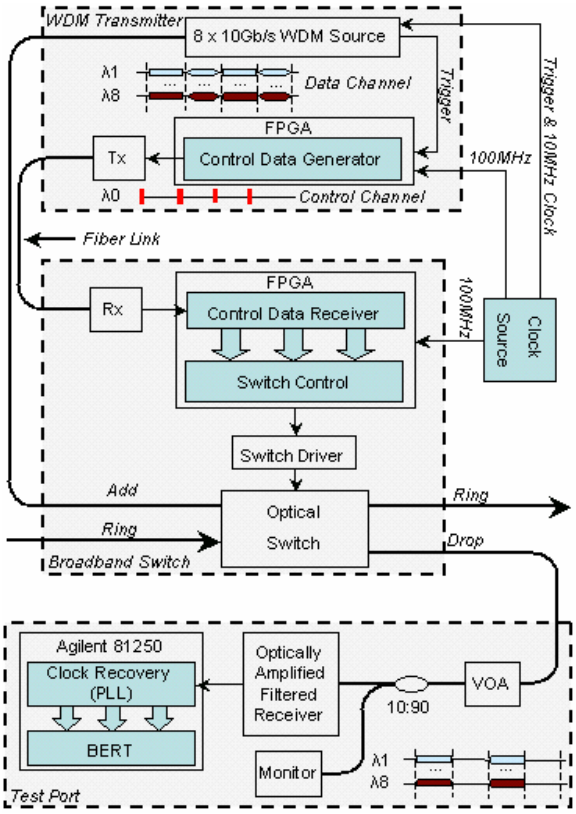


Fig.2. Experimental Set-up

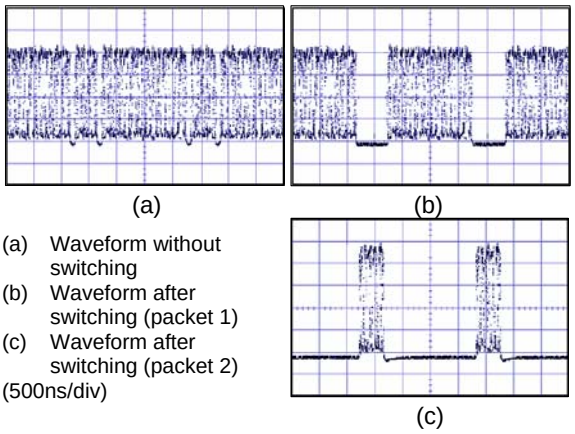
Experimental Set-up

The experimental set-up to implement FPGA control is shown in Fig.2. One Xilinx Spartan II FPGA is partitioned and used to perform processing functions for both the transmitter and the switch. Once a packet is initiated, the FPGA generates the routing information for the corresponding packet including preamble, destination address and slot delimit. This routing information travels in a control channel to the switch node where it is read by the switch control part of the FPGA. The control information precedes the packet payload to allow processing time and facilitate low latency networking. The FPGA generates two

trigger signals to delimit the beginning and the end of the switched time slot. A switch driver waveform is subsequently generated to instruct the broadband slot switch to route the desired multiwavelength packet.

At the data transmitter, eight distributed feedback lasers operating at wavelengths from 1547.7nm to 1553.4nm are multiplexed and amplified. The WDM signal is data modulated using a 10Gbits/s Pulse and Pattern Generator (PPG). The pattern comprises two interleaved packets with durations 1.5µs and 0.4µs and a guardband of 76.8ns between. The duration of the guardband is limited by the timing jitter of the switching signal from the FPGA, although this jitter may be reduced by increasing the clock speed of the FPGA. A 30 byte clock assist preamble is included at the beginning of each packet and 2^{13}-1 pseudo random binary sequences are employed for the packet payloads.

An Agilent 81250 error test set with an internal phase lock loop (PLL) is used to assess power penalty due to switching. An optically preamplified receiver is used with an AWG for consecutive testing of the wavelength channels.



(a) Waveform without switching
(b) Waveform after switching (packet 1)
(c) Waveform after switching (packet 2)
(500ns/div)

Fig.3. Waveforms with and without switching

Two commercially available switches are assessed: a 2x2 MZ (Aeroflex) switch and an SOA (Kamelian) switch. The observed waveforms with and without switching are shown in Fig.3. The switch is used to drop the desired packet, while the remaining packet sequence passes out to the ring.

Experimental Results

Stable, error free operation is demonstrated for all eight channels under routing operation with no evidence of noise floors. Measurements for back-to-back and routed performance are shown in Fig.4 for the 1552.6nm channel.

For the MZ switch, the incurred penalty is 0.2 dB. An additional penalty due to routing operation of 2.3 dB is measured for both MZ and SOA switches. This penalty is dominated by the clock recovery and synchronization of the received packet, and the control signal to the switch is not believed to cause a

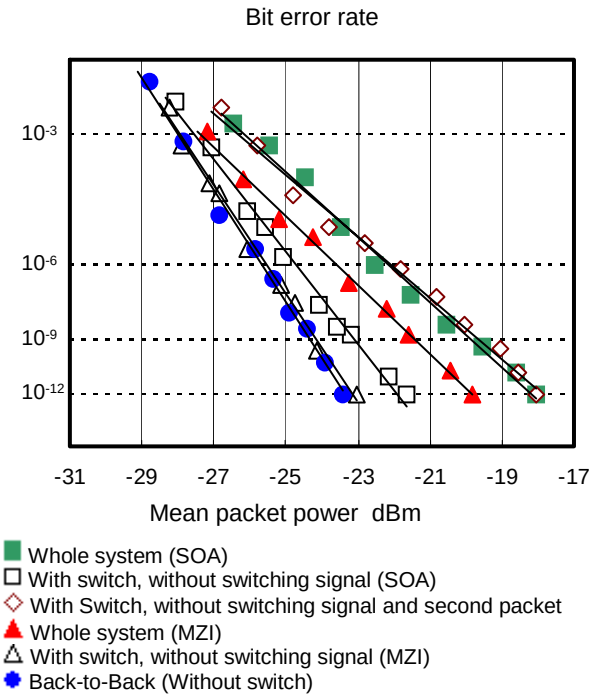


Fig.4. BER for MZ and SOA switches

significant penalty. This is verified by measuring the BER performance without driving the optical switch and without transmitting the second packet. A 2.1dB penalty purely attributable to clock recovery is measured indicating a 0.2 dB optical switching penalty. The SOA switch causes an extra 1.3 dB penalty compared with the MZ switch at the high power used in this measurement. The difference should be reduced for lower input optical powers.

Conclusions

A FPGA based low rate control scheme (100Mb/s) is proposed and demonstrated to route high rate WDM optical packet (80Gb/s). 0.2 dB penalty is observed due to the optical routing while a 2.1 dB penalty is attributable to electrical clock recovery and synchronization. Implementation of control and data over the same fibre link will be reported at the conference.

Acknowledgement

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